



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,276	01/14/2002	Goro Nakatani	040894-5755	4701

9629 7590 03/11/2005

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER


IM, JUNGHWA M

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/043,276	Applicant(s) NAKATANI ET AL. 	
	Examiner Junghwa M. Im	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3 and 8-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3 and 8-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>07/07/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

Claims 1 and 8 are objected to because of the following informalities: claims 1 and 8 recite a limitation of “a planarized polyimide” and “a polyimide resin layer” as if they are two different layers. However, the instant invention explicitly discloses that there is only one polyimide layer.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 8 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Harada et al. (US 6476491), hereinafter Harada.

Regarding claim 1, Fig. 7F of Harada shows semiconductor device comprising:

a first interconnect layer (66) arranged above a substrate (1) on which a functional semiconductor region (6) is formed;

an inter layer dielectric (201a, 201b) covering a surface of the first interconnect layer;

Art Unit: 2811

a silicon nitride film (201c; col. 13, lines 50-55) formed so as to cover entirely a top surface of said interlayer dielectric,

a metal interconnect layer (208) covering over said silicon nitride film, said metal interconnect layer being consist of gold material (col. 14, lines 38-40); and

a planarized polyimide (207; col. 14, line 49) formed on the metal interconnect layer,

wherein the polyimide layer is removed at a part of a region of the metal interconnect layer and a bond wire (209) is connected to the region of the metal interconnect layer.

Regarding claim 3, Harada discloses that the insulating layers are deposited by plasma CVD method (col. 1, lines 34-35).

In addition, “high-density plasma CVD” is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 8, Fig. 7F of Harada shows a semiconductor device comprising:

a first interconnect layer (66) covering a first portion of a surface of a functional semiconductor region (1);

an inter layer dielectric (201a, 201b) covering a second portion of the surface of the functional semiconductor region and a portion of a surface of said first interconnect layer, thereby forming a contacting hole on the surface of the first interconnect layer;

a silicon nitride film (201c; col. 13, lines 50-55) covering a top surface of said inter layer dielectric around the contacting hole on the surface of the first interconnect layer;

Art Unit: 2811

a barrier layer (204a in Fig. 7C) covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region (col. 14, lines 1-10) ;

a metal interconnect region (208) consist of gold material (col. 14, lines 38-40) covering over the barrier region, thereby forming a metal interconnect region; and

a planarized polyimide (207; col. 14, line 49) covering the metal interconnect layer and the silicon nitride surface around the metal interconnect region

wherein the polyimide layer is removed at a part of a region of the metal interconnect layer and a bond wire (209) is connected to the region of the metal interconnect layer.

Regarding claims 10 and 11, Harada discloses the first interconnect layer consists of aluminum (col. 24, lines 31-32).

Regarding claim 12, Harada discloses the inter layer dielectric consists of USG film (201b, siliconoxide; col. 13, lines 52-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada in view of Toyosawa et al. (US 6441467), hereinafter Toyosawa.

Art Unit: 2811

Regarding claim 9, Fig. 7F of Harada shows substantially the entire claimed structure except “the barrier layer consists of titanium.” Toyosawa discloses that the barrier layer consists of titanium (col. 7, lines 48-50).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Toyosawa to the device of Harada in order to have the barrier layer consisted of titanium to diffusion of the metallic compound to the neighboring layer while using the well-known barrier material.

Regarding claim 13, Fig. 7F of Harada shows the functional semiconductor region further comprises a gate (4) isolated from the first interconnect layer by a second dielectric layer (55, 59, 63), wherein the first interconnect layer is connected to the gate through a contacting area disposed within the second dielectric layer, however, fails to show a polysilicon gate. Fig. 1 of Toyosawa shows the functional semiconductor region further comprises a gate (3) isolated from the first interconnect layer by a second dielectric layer (10), wherein the first interconnect layer is connected to the gate through a contacting area disposed within the second dielectric layer

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Toyosawa to the device of Harada in order to have a polysilicon gate since the polysilicon is well known material used for a gate.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2811

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2811

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800